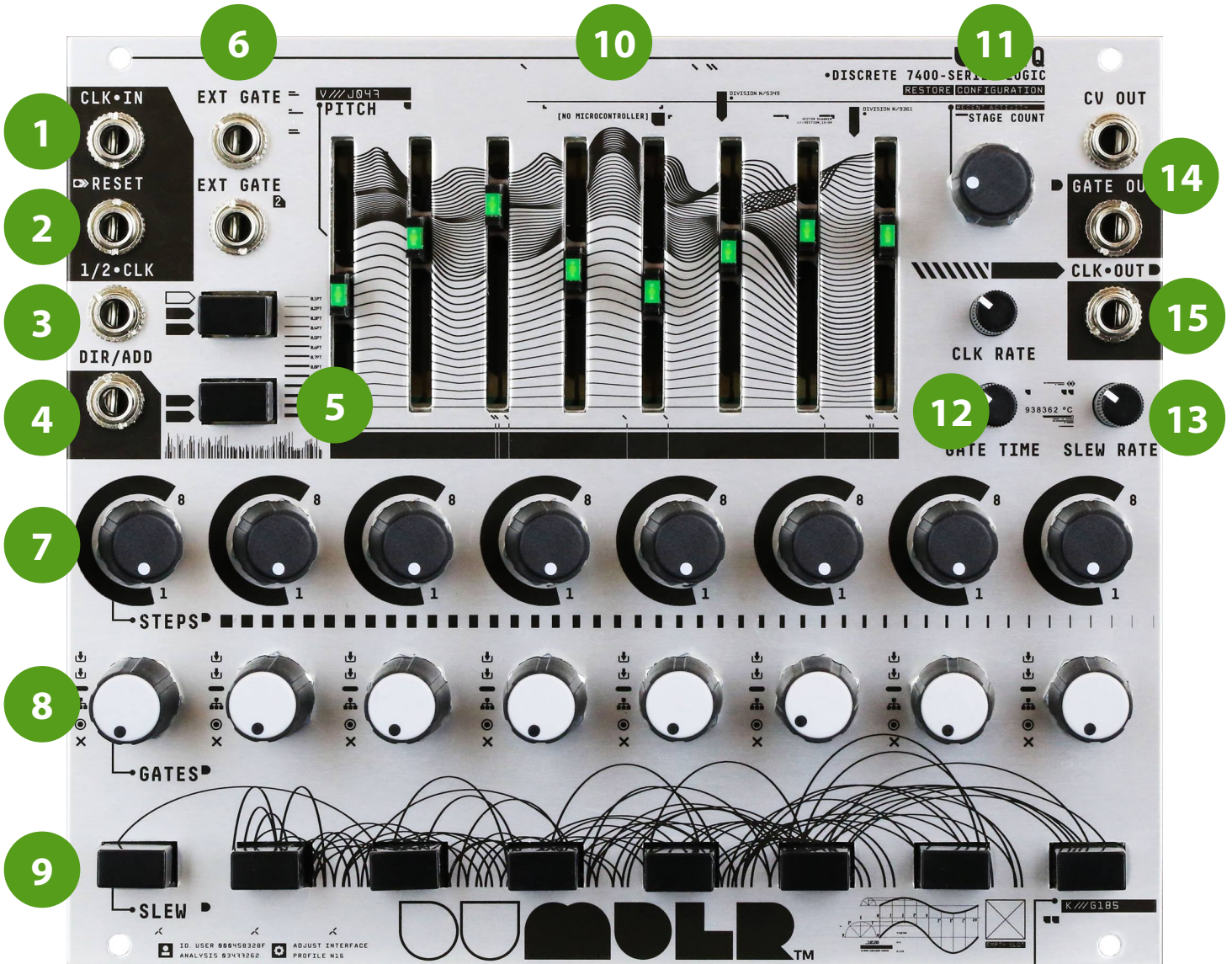










# • DISCRETE 7400-SERIES LOGIC



Width: 30HP · Depth: 35mm · Current draw: 8 mA +12V / 8 mA -12V / 110 mA 5V



- 1 Clock input**  
When connected, this signal replaces the internal clock. DU-SEQ uses the precise timing of the clock input for stage/step counting, and the actual pulse width as the gate time.
- 2 Reset input**  
When triggered, DU-SEQ returns to the left-most stage (stage 1).
- 3 1/2 Clock input & button**  
When the input is gated or the switch is set on, DU-SEQ runs at half the clock rate (with the clock output still at the full rate).
- 4 Direction/Address input**  
In Direction mode, when gated, DU-SEQ counts through stages in reverse. In Address mode, allows CV selection (0 – 5 volt range) of stage.
- 5 Direction/Address mode switch**  
Toggles between Direction (off) and Address (on) mode.
- 6 External Gate inputs**  
Gate signals used when the gate mode is set to external. The second gate input mirrors the first when disconnected. External gates are, in general, independent of the clock.
- 7 Step Count switches**  
Specify the number of steps (1 – 8) to count at the associated stage.
- 8 Gate Type switches**  
Specify the type of gate to use at the associated stage (see legend).
- 9 Slew Rate Limiter switches**  
When set on, enable slew rate limit at the associated stage (when coming from another stage).
- 10 Pitch sliders**  
Select the pitch (two octave range) for the associated stage. The green LED indicates gate output for that stage.
- 11 Stage Count switch**  
Specify the number of stages (1 – 8) to enable, starting with the left-most stage (stage 1).
- 12 Clock Rate & Gate Time knobs**  
Set the internal clock rate and internal gate pulse width.
- 13 Slew Rate knob**  
Control the slew rate used by stages with slew rate limit enabled.
- 14 Pitch CV & Gate outputs**  
Output pitch control voltage (0 – 2V range) and gate signal, respectively.
- 15 Clock output**  
Outputs the clock used by DU-SEQ (internal or external).

-  External Gate 2
-  External Gate 1
-  Long Gate
-  Multiple Gate
-  Single Gate
-  No Gate